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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,630	09/22/2003	Hyeong-Seob Kim	SEC.1064	7303

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/665,630	KIM ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *33-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,9-18 and 21-30* is/are rejected.

7)☒ Claim(s) *4,5,7,8,19,20,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated January 31, 2005, Applicant has elected Invention I, claims **1-32**, drawn to a device without traverse is acknowledged. Accordingly, claims **33-48** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **33-38**, drawn to a method.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREA, 2003-18446 on 03/25/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 09/22/2003. The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected for the following reason.

Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **1, 12-16, 29 and 30** are rejected under 35 U.S.C. 102(a,e) as being anticipated by Yanagida (USP: 6,429,096), Applicant's submitted prior art (ASPA).

Regarding claim **1**, Yanagida discloses in Figs. 5A-8, and the corresponding texts as set forth in column 6, line 20-column 10, line 43, a semiconductor chip package, comprises:

a semiconductor chip 1, 7 which includes a through hole 8a extending there through from an active first surface to an inactive second surface;

a first conductive pad 2 which at least partially surrounds the through hole on the active first surface of the semiconductor chip;

a printed circuit board 25 which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a conductive pad 11 aligned with the through hole the semiconductor chip; and

a conductive material 23 which fills the through hole and contacts the first and second conductive pads.

Regarding claims **12-13 and 29-30**, Yanagida discloses in Fig. 8 a semiconductor chip package further comprising an adhesive layer/an anisotropic conductive film 9 interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board.

Regarding claim **14**, Yanagida discloses in Figs. 5A-8 a semiconductor chip package further comprises a protective layer 8, 28 covering the active first surface of the semiconductor chip.

Regarding claim **15**, Yanagida discloses in Figs. 5A-8, and the corresponding texts as set forth in column 6, line 20-column 10, line 43, a semiconductor multi-package stack, comprises:

a plurality of stacked semiconductor chip packages, each chip package comprising (a) a semiconductor chip 1, 7 which includes a through hole 8a extending there through from an active first surface to an inactive second surface; (b) a first conductive pad 2 which at least partially surrounds the through hole on the active first surface of the semiconductor chip; (c) a printed circuit board 25 which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a conductive pad 11 aligned with the through hole the semiconductor chip; and (d) a conductive material 23 which fills the through hole and contacts the first and second conductive pads.

Regarding claim **16**, Yanagida discloses in Fig. 5A-8 the semiconductor chip packages are stacked such that the conductive material of a lower chip package contacts the printed circuit board of an adjacent upper chip package.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **2-3, 17, 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagida (USP: 6,429,096) in view of Wu et al. (USP 6,459,150 hereinafter referred to as "Wu").

Yanagida discloses all the claimed limitations except for the conductive material comprises solder, and wherein the solder forms a solder bump over the active first surface of the semiconductor chip. Wu teaches in Fig. 2G a semiconductor package comprises the solder material used to fill up aperture 70 and formed the conductive plugs 92, and the solder forms a solder bump 100 over the active first surface of the semiconductor chip 62 (col. 8, lines 39-63). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the solder material to fill up aperture and formed the conductive plugs, and the solder forms a solder bump over the active first surface of the semiconductor chip, as taught by Wu in order to effectively bonds the plurality of conductive pads on the silicon wafer to the plurality of conductive pads on the electronic substrate (col. 8, lines 51-55).

Claims **6, 9, 10, 21-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagida (USP: 6,429,096) in view of Saito et al. (USP 6,735,857 hereinafter referred to as "Saito").

Yanagida discloses all the claimed limitations except for the printed circuit board includes an aperture aligned below the second conductive pad opposite the through hole, and further comprises an electrode/a solder ball which is electrically connected to the second conductive pad and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board. Saito teaches in Figs 6-7 a printed circuit board 7 includes an aperture aligned below the second conductive pad 1 opposite the through hole 8, and an electrode/solder ball 6 which is electrically connected to the second conductive pad and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board (col. 5, lines 37-67). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the printed circuit board including an aperture aligned below the second conductive pad opposite the through hole, and an electrode/solder ball which is electrically connected to the second conductive pad and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board, as taught by Saito in order to form solder balls for external connections.

Claims **11, 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagida (USP: 6,429,096) in view of Hayasaka et al. (USP 6,809,421 hereinafter referred to as "Hayasaka").

Yanagida discloses all the claimed limitation except for a semiconductor chip package further comprises an insulating layer located on sidewalls of the through hole of the semiconductor chip. Hayasaka teaches in Fig. 4 a multichip semiconductor device comprises an insulating layer 5 located on sidewalls of the through hole of the semiconductor chip 1. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an insulating layer located on sidewalls of the through hole of the semiconductor chip, as taught by Hayasaka in order for insulation between a metal plug and a substrate.

Allowable Subject Matter

Claims **4, 5, 7, 8, 19, 20, 31 and 32** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Yanagida, Wu, Hayasaka and Saito, taken alone or in combination, fail to teach the claimed limitation a semiconductor chip package wherein the conductive material comprises a metal plug which protrudes into the through hole from the second conductive pad of the printed circuit board, and solder which surrounds the metal plug as recited in claim **4**; a semiconductor multi-package stack wherein the conductive material of each semiconductor chip package comprises a metal plug which protrudes into the through hole from the second conductive pad of the printed circuit board, and solder which surrounds the metal plug as recited in claim **19**; and a semiconductor multi-package stack further comprises an external printed board having a first

conductive pad formed on a first surface and a second conductive pad formed on an opposite second surface, and further has an external electrode attached to the second conductive pad, wherein the conductive material of the bottommost semiconductor chip package is attached to the first conductive pad of the external printed circuit board, and wherein the first and second conductive pads of the external printed circuit board are electrically connected as recited in claim **31**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

02/24/05

Andy Huynh

Patent Examiner